Notice of Allowability	Application No.	Applicant(s)	
	10/042,924	FORBES, LEONARD	
	Examiner	Art Unit	
	William C. Vesperman	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *10/6/2004*.

2. ☒ The allowed claim(s) is/are *1-6 and 21-49*.

3. ☒ The drawings filed on *08 March 2004* are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date 3-4-04and 6-1-04
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

1. This action is in reply to applicant's RCE of 10/06/2004.

Allowable Subject Matter

2. Claims 1 - 6, 21 - 49 are allowed.

3. The following is an examiner's statement of reasons for allowance.

Hsu et al. (US 6,245,613) teaches (Figure 17) a method of forming a field effect transistor which includes: forming an oxide layer of 10 to 40 Angstroms on and contacting a substrate; forming a channel region separating the source and drain region in the substrate; forming a floating gate on and contacting the oxide layer; forming a dielectric layer on the floating gate; and forming a control gate on dielectric layer.

Hsu et al. does not teach forming an enhancement mode p-channel memory cell. In addition, Hsu et al. does not teach an oxide layer which contacts the substrate, the source, the drain and the channel regions; and wherein the p-channel memory cell is adapted to erase using a potential of magnitude of about 3 volts or less applied to the floating gate or that the enhancement mode p-channel memory cell has an operating voltage of less than 2.5 volts across the oxide layer.

Claims 1 – 6, 21 - 23

The prior art does not teach or suggest in combination with the other claimed limitations, a method of forming an enhancement mode p-channel memory cell which includes: forming an oxide layer of less than 40 Angstroms on and

contacting a substrate in which the oxide layer contacts the source, drain and channel regions; and wherein the p-channel memory cell is adapted to erase using a potential of magnitude of about 3 volts or less applied to the floating gate or having an operating voltage of less than 2.5 volts across the oxide layer.

Claims 24 - 29

The prior art does not teach or suggest in combination with the other claimed limitations, a method of forming an enhancement mode p-channel memory cell which includes: forming an oxide layer of less than 40 Angstroms on and contacting a substrate in which the oxide layer contacts the source, drain and channel regions; and wherein the p-channel memory cell is adapted to have a reliability of a number of cycles of performance of approximately 10 to the twelve to 10 to the fifteen cycles over a life time of the enhancement mode p-channel memory cell; and having an operating voltage of less than 2.5 volts across the oxide layer.

Claims 30 - 32

The prior art does not teach or suggest in combination with the other claimed limitations, a method of forming an enhancement mode p-channel memory cell which includes: forming an oxide layer of less than 30 Angstroms on and contacting a substrate in which the oxide layer contacts the source, drain and channel regions; and wherein the p-channel memory cell is adapted to erase using a potential of magnitude of about 3 volts or less applied to the floating gate.

Claims 33 – 35

The prior art does not teach or suggest in combination with the other claimed limitations, a method of forming an enhancement mode p-channel memory cell which includes: forming a plurality of memory cells, wherein at least one p-memory is formed and wherein one p-memory cell includes: forming an oxide layer of less than 23 Angstroms on and contacting a substrate in which the oxide layer contacts the source, drain and channel regions; and having an operating voltage of approximately 1.0 volt applied to the control gate; and forming at least one sense amplifier that is coupled to the plurality of memory cells.

Claims 36 – 40

The prior art does not teach or suggest in combination with the other claimed limitations, a method of forming an enhancement mode transistor which includes: forming an oxide layer of less than 40 Angstroms on and contacting a substrate in which the oxide layer contacts the source, drain and channel regions; forming a floating gate on and contacting the oxide layer, wherein forming the floating gate includes forming a floating gate which is adapted to hold a charge on the order of 10 to the seventeen Coulombs for longer than 1.0 hour at 20 degrees Celsius; forming a dielectric layer on the floating gate where the dielectric layer includes silicon dioxide; and forming a control gate on the dielectric layer.

Claims 41 - 46

The prior art does not teach or suggest in combination with the other claimed limitations, a method of forming an enhancement mode p-channel memory cell which includes: forming a plurality of memory cells, wherein at least one p-

memory is formed and wherein one p-memory cell includes: forming an oxide layer of less than 40 Angstroms on and contacting a substrate in which the oxide layer contacts the source, drain and channel regions; forming a floating gate on and contacting the oxide layer wherein the floating gate is adapted to hold a charge on the order of 10 to the seventeen Coulombs for longer than 1.0 hour at 20 degrees Celsius; and forming at least one sense amplifier that is coupled to the plurality of memory cells.

Claims 47 - 49

The prior art does not teach or suggest in combination with the other claimed limitations, a method of forming an enhancement mode p-channel transistor which includes: forming an oxide layer of less than 23 Angstroms on and contacting a substrate in which the oxide layer contacts the source, drain and channel regions; and forming a floating gate on and contacting the oxide layer wherein the floating gate is adapted to hold a charge on the order of 10 to the seventeen Coulombs for longer than 1.0 second at 85 degrees Celsius.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Ying Shi, Xiewen Wang and T. P. Ma, Tunneling Leakage Current in Utrathin Nitride/Oxide Stack Dielectrics (Published IEEE, 1998, pages 388 – 390) teaches using a ultra-thin nitride/oxide stack comprising of a SiN layer and a SiO2 layer formed over the SiN layer in order to replace a conventional oxide insulating layer.

Yang et al. (US 6,515,328) teaches a semiconductor devices with reduced control gate dimensions.

Yang et al. (US 6,383,939 B1) teaches a method of etching a memory gate stack.

Chang et al. (US 2003/0001197 A1) teaches a method for forming a memory cell having a contoured floating gate.

Chuang et al. (US 5,869,370) teaches forming a thin tunneling oxide layer using CVD.

Chung (US 2003/0201491 A1) teaches a semiconductor device containing oxide/nitride/oxide insulating stack layers.

Chang (US 5,408,115) teaches a self aligned EEPROM device.

Wu (US 6,316,316) teaches a method of forming high density flash memories.

Lin et al. (US 6246089) teaches flash EEPROM devices.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to William C. Vesperman whose telephone number is 571-272-1701. The examiner can normally be reached on Mon. - Fri., 8:00 - 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr. can be reached on 571-272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

WCV

Art Unit 2813

October 22, 2004

C. Chaudhari

Chandra Chaudhari
Primary Examiner